

STF 522: TDL Phase 4

Status Report

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Document History

- 2017-05-31: Document submitted for MTS#71
- 2017-05-11: Document submitted for SG#2
- 2017-02-27: Document submitted for SG#1
- 2017-01-25: Document submitted for MTS#70

From the Terms of Reference...

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TDL Phase 4: Objectives

- New Part 6 for mapping TDL to TTCN-3
- Adaptation and extension of MM addressing CRs
 - new test configuration features (clarifications needed)
 - related to the mapping to TTCN-3
- Adaptation and extension of GR, XF, TO
- New Part 5 to relocate the UML profile (currently annex to MM)
- Requirements for security and performance testing with TDL (TR)

TDL Phase 4: Deliverables

Deliv.	Work Item code Standard number	Working title Scope
D1	RES/ES 203 119-1 V1.4.1	Test Description Language; Meta-Model and Semantics Scope: common concepts, meta-model, semantics
D2	RES/ES 203 119-2 V1.3.1	Test Description Language; Graphical Syntax Scope: TDL graphical concrete syntax for end users
D3	RES/ES 203 119-3 V1.3.1	Test Description Language; Exchange Format Scope: TDL exchange format for tool interoperability
D4	RES/ES 203 119-4 V1.3.1	Test Description Language; Structured Test Objective Specification Scope: TDL extension for structured test objectives
D5	DES/ES 203 119-5 V1.1.1	Test Description Language; UML profile for TDL Scope: TDL to UML meta-model mapping
D6	DES/ES 203 119-6 V1.1.1	Test Description Language; Mapping of TDL to TTCN-3 Scope: Mapping rules to automatically generate TTCN-3 test case skeletons from TDL test descriptions
D7	DTR/ MTS-1029504TDLSecPerfReq	TDL and its usage for security and performance testing; consolidated requirements (technical report)

Status Update

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Task 0: Work Plan

- Timescale: Jan, 2017 (+4 months) Jan, 2018 (+1 month)
 - delays due to administrative overhead at respective organisations
 - final confirmation received on Dec 15, 2016
 - work remotely, meet in person only if necessary
 - coordinated remote sessions scheduled as needed, based on availability
- Working sessions planned so far, further sessions as needed
 - WK7: Feb 14-17 Session 1 @ UG (4 days)
 - TBC: Sept/Oct: Session 2 (4-5 days, in planning)

Task 0: Milestones (Current Planning)

Ν	Task / Milestone / Deliverable	ToR Targets	Current Targets				
MO	Start of work	Sep-2016	Jan-2017				
Т0	Project management	Sep-2016-Sep-2017	Jan-2017–Jan-2018				
T1	TDL-to-TTCN-3 mapping	Sep-2016-Sep-2017	Jan-2017–Jan-2018				
T2	Advanced test configuration features	Sep-2016–Apr-2017	Jan-2017–Aug-2017				
Т3	Language maintenance	Sep-2016–Apr-2017	Jan-2017–Aug-2017				
T4	Requirements for security and performance testing	Mar-2017-Sep-2017	Jun-2017–Dec-2017				
M1	Informal report on planning	16-Dec-2016	Jan-2017				
M2	1 st drafts	28-Apr-2017	May-2017				
М3	2 nd drafts	28-Jul-2017	Sep-2017				
M4	Final drafts for MTS review	01-Sep-2017	Dec-2017				
M5	Final report, end of work, TB approval	27-Sep-2017	Jan-2018				
M6	Membership vote	27-Sep-2017	Feb-2018				
M7	Publication	01-Dec-2017	Apr-2018				

Task 0: Overall Timeline (Current)

Task Milest.	Description	J	F	Μ	Α	Μ	J	J	Α	S	0	Ν	D	J	F	Μ	Α
TO	Project management																
T1	TDL-to-TTCN-3 mapping																
T2	Advanced test configuration																
T3	Language maintenance																
T4	Requirements solicitation																
MO	Start of work																
M1	Informal report on planning																
M2	1st drafts																
M3	2nd drafts																
M4	Final drafts for MTS review																
M5	Final report, TB approval																
M6	Membership vote																
M7	Publication																

Notes from SG Meetings

- Inter-SUT communication remains as future work
- Introduce local ordering as explicit property of test description
- Focus on message-based communication at first
- Data mapping required at first
- Advanced test configuration as TDL extension (similar to TO)

Notes from SG Meetings

- Advanced test configurations
 - integrated, self-contained -> separate extension (new WI) or annex
 - additional discussion on generic notion of inheritance throughout TDL
- Unexpected behaviour
 - minimal base solution + recommendations
 - focus on what is specified in TDL and not on what is not
- Implementation of mapping
 - under TOP? with STF resources?

Deliverable Planning

- Focus on Part 1, 5 and 6 for Milestone 1
 - Parts 2, 3, 4 need to be updated according to changes in Part 1
 - changes in Part 1 need to be approved and validated first
- Examples in all parts need to be updated and aligned

Status: Part 1

- Extracted Annex C into Part 5
- Added support for local ordering (constraints pending)
- Added support for collections
- Added support for procedure-based communication
- Added proposal for extended test configurations (Annex C)

Status: Part 6

- Partial mapping specifications (updates for new features pending)
- Mappings only for local ordering
- Contents from Part 1 copied for reference
 - will be removed once mappings for an element are done
- Examples

Type PDU; Type ACK ; Type C_RNTI; Type PDCCH (optional c_rnti of type C_RNTI); Type CONFIGURATION;

PDU mac_pdu ;
ACK harq_ack ;
C_RNTI ue;
C_RNTI unknown;
PDCCH pdcch;
CONFIGURATION RRCConnectionReconfiguration ;

type charstring SimpleType; type float Second; type SimpleType PDU; type SimpleType ACK; type SimpleType C_RNTI;

```
type record PDCCH {
   C_RNTI c_rnti optional
}
```

type SimpleType CONFIGURATION;

```
template PDU mac_pdu := "mac_pdu"; // some value is needed
template ACK harq_ack := "harq_ack";
template C_RNTI ue := "ue";
template C_RNTI unknown := "unknown";
template PDCCH pdcch := {};
template CONFIGURATION RRCConnectionReconfiguration :=
    "RRCConnectionReconfiguration";
```

```
Gate Type defaultGT accepts
                                                 type port defaultGT_to_map message {
   ACK, PDU, PDCCH, C_RNTI, CONFIGURATION;
                                                   //this is a port type for SUT-Tester connections
                                                   inout charstring, PDCCH /* ACK, PDU, C_RNTI, CONFIGURATION ; */
Component Type defaultCT having {
                                                 }
    gate g of type defaultGT;
}
                                                 type port defaultGT_to_connect message {
                                                   //this is a port type for Tester-Tester connections
Test Configuration defaultTC {
                                                   inout charstring, PDCCH /* ACK, PDU, C_RNTI, CONFIGURATION ; */
    create Tester SS of type defaultCT;
                                                 }
    create SUT UE of type defaultCT ;
    connect UE.g to SS.g;
                                                 type component MTC_CT {
                                                   //component type for MTC
}
                                                   //variable for the PTC(s) --TESTER component(s) in TDL
                                                   var defaultCT TESTER_SS;
                                                 }
                                                 type component defaultCT {
                                                   port defaultGT_to_map g_to_map;
                                                   port defaultGT_to_connect g_to_connect;
                                                 }
                                                 function defaultTC() runs on MTC_CT {
                                                   // Test Configuration defaultTC, behaviour to be extracted
                                                   TESTER_SS := defaultCT.create;
                                                   map (TESTER_SS:g_to_map, system:g_to_map);
                                                   TESTER_SS.start(behaviour0fTESTER_SS());
```

```
altstep to_handle_deviations_from_TDL_description_AS () {
 [] any port.receive {
   setverdict(fail);
   //QUESTION TO SG: in case of deviation shall we stop the test case?
   mtc.stop;
  }
 //here can also be handled if nothing arrives, but in this case a timer shall be started
 //before every receive instruction and the timer must be handled somehow
 //or we can leave the timeout for the execute instruction called with the optional
 //timer parameter - but in this case the final verdict will be 'error'
}
altstep quiescence_handler_AS (timer quiescence) {
 //for all guiescence that is not connected to a gate
 [] any port.receive{
    setverdict(fail);
    //OUESTION TO SG: in case of deviation shall we stop the test case?
    mtc.stop;
   }
  [] quiescence.timeout {
    setverdict(pass);
  }
}
```

```
Test Description TD_7_1_3_1
  uses configuration defaultTC {
    perform action preCondition:
    perform action preamble;
    SS.g sends pdcch (c_rnti=ue) to UE.g;
    SS.g sends mac_pdu to UE.g;
    UE.g sends harg_ack to SS.g with {
        test objectives : TP1 ;
    };
    set verdict to PASS ;
    SS.g sends pdcch (c_rnti=unknown) to UE.g;
    SS.g sends mac_pdu to UE.g;
    //Interpolated original step 6 into
   //an alternative behaviour, covering both
   //the incorrect and the correct behaviours
                                                   alt{
    alternatively {
        UE.g sends harq_ack to SS.g;
        set verdict to FAIL ;
                                                      }
    } or {
        gate SS.g is quiet for five ;
        set verdict to PASS ;
                                                   }
    } with {
                                                  }
       test objectives : TP2 ;
    }
}
```

function behaviourOfTESTER_SS() runs on defaultCT {
 timer quiescence;

activate(to_handle_deviations_from_TDL_description_AS());

```
g_to_map.send(modifies pdcch := {c_rnti := ue})
// multiple level modifications cannot be handled in this way
g_to_map.send(mac_pdu);
g_to_map.receive(harq_ack);
/*Test Objective Statisfied: TP1 */
setverdict(pass);
```

```
g_to_map.send(modifies pdcch := {c_rnti := unknown});
// multiple level modifications cannot be handled in this way
g_to_map.send(mac_pdu);
quiescence.start(five);
alt{
    [] g_to_map.receive(harq_ack){
        setverdict(fail);
    }
    [] quiescence_handler_AS(quiescence);
    /*Test Objective Statisfied: TP2 */
}
```

```
Test Description TD_7_1_3_1
                                                  testcase TD_7_1_3_1() runs on MTC_CT
  uses configuration defaultTC LOCALLY ORDERED {
                                                      system defaultCT // It works if there is only one SUT
    perform action preCondition:
                                                  {
    perform action preamble;
                                                    preCondition();
                                                    preamble()
    SS.g sends pdcch (c_rnti=ue) to UE.g;
    SS.g sends mac_pdu to UE.g;
                                                    activate(to_handle_deviations_from_TDL_description_AS());
    UE.g sends harg_ack to SS.g with {
        test objectives : TP1 ;
                                                    //Test Configuration defaultTC(), behaviour to be extracted
    };
                                                    defaultTC();
    set verdict to PASS ;
    SS.g sends pdcch (c_rnti=unknown) to UE.g;
                                                   all component.done;
    SS.g sends mac_pdu to UE.g;
                                                  }
    //Interpolated original step 6 into
   //an alternative behaviour, covering both
   //the incorrect and the correct behaviours
    alternatively {
        UE.g sends harq_ack to SS.g;
        set verdict to FAIL ;
    } or {
        gate SS.g is quiet for five ;
        set verdict to PASS ;
    } with {
       test objectives : TP2 ;
    ł
}
```

Communications

- Proposals for UCAAT (presentation and/or tutorial)
 - other TDL-related contributions submitted to UCAAT
- Interest in UP4TDL from S. Maag / TSP
- Discussions via official channels
 - official policy to use only official channels
 - private mails disregarded in the future
- Discussion regarding positioning and marketing of TDL
- Discussions regarding TOP

Any other business?

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