

10th UCAAT

User Conference on
Advanced Automated Testing

Parallel Boundary Scan & Programming testing solution. An application for PCB structural integrity evaluation.

Raul IONEL



16/11/2023



Content

Context – solution implementation.

- Request from industry and solution guidelines.

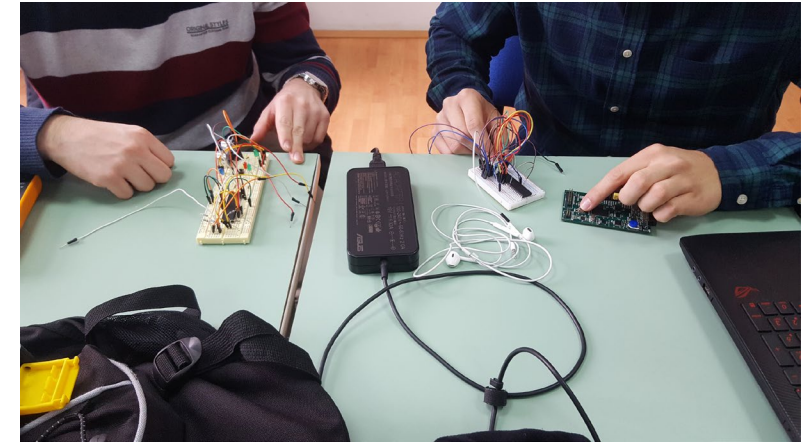
Why Boundary Scan (IEEE 1149.1) Testing?

- Intro concepts;
- An evaluation vs. other testing methods.

The application.

- BST integration considerations;
- Deployment;
- Results.

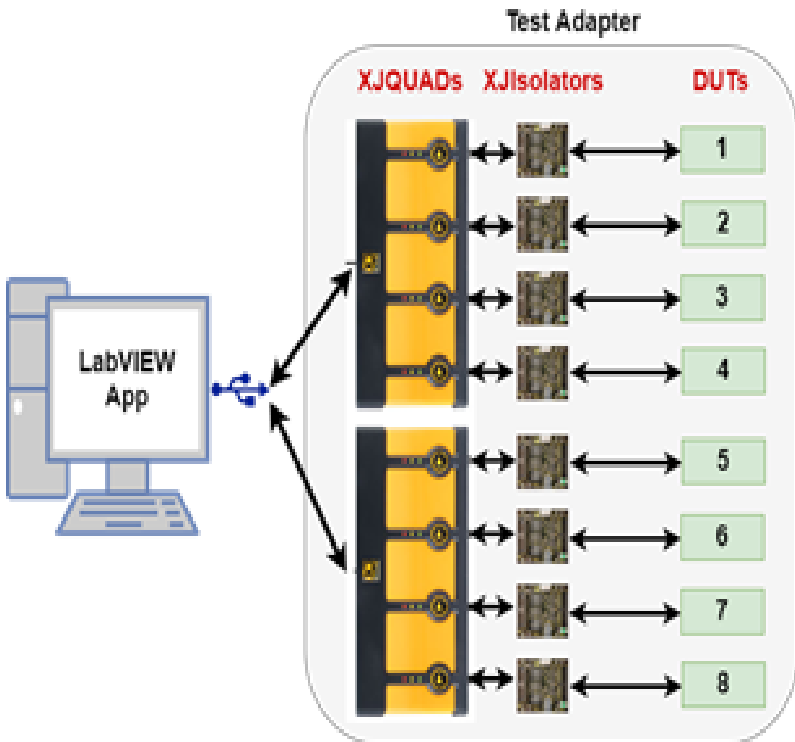
Conclusions and future work.



Acknowledgement – The authors are grateful to XJTAG (xjtag.com) and Alfa Test (alfatest.ro) for the support of the Design for Boundary Scan lecture/laboratory at the Politehnica University Timișoara.

Context – solution implementation

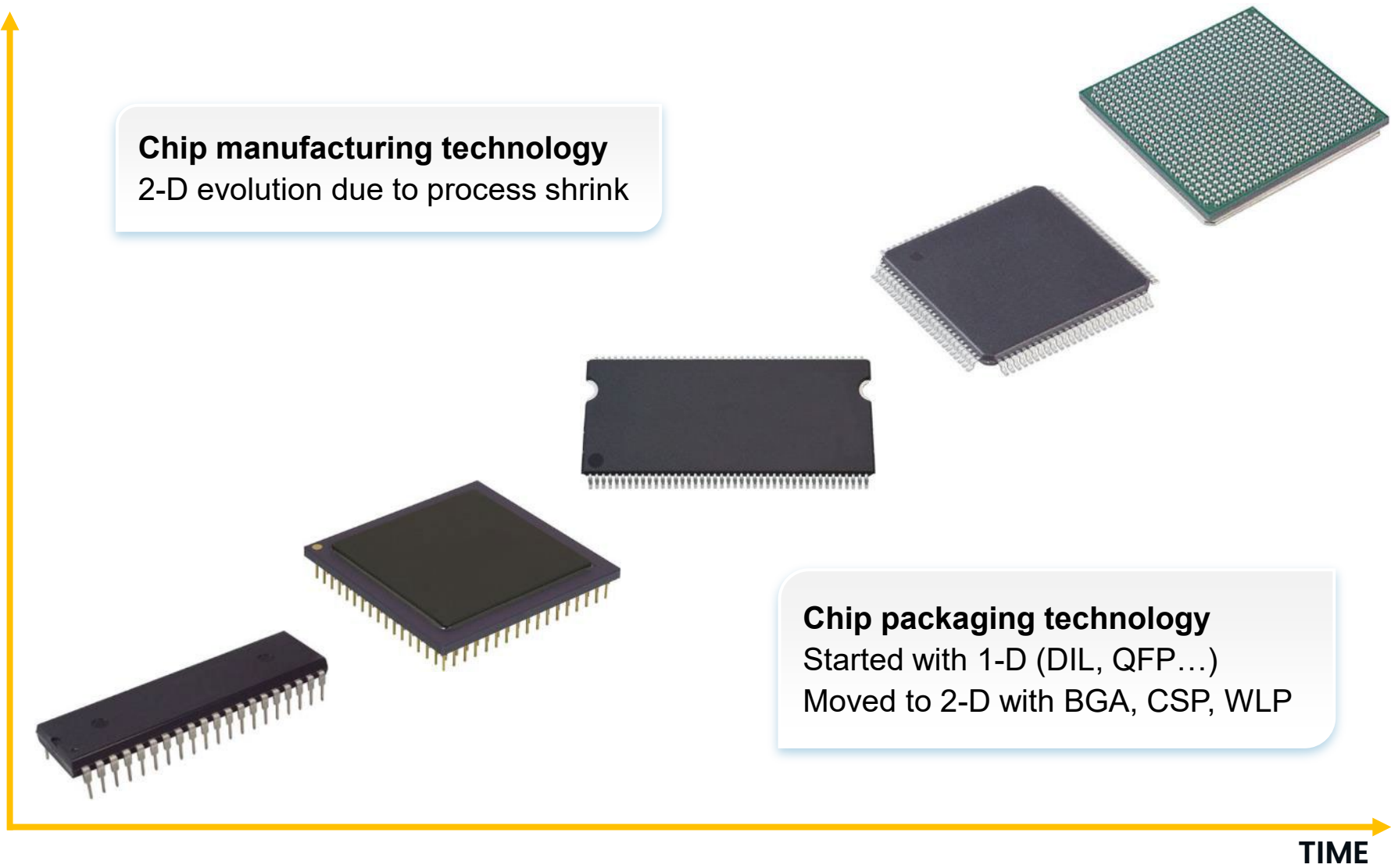
Request from industry and solution guidelines.

| Existing solution | Proposed solution | Improved features |
|--|---|---|
| <ul style="list-style-type: none"> - Request from one important industry partner acting in life & safety products development; - Solution used for BST & Programming of a single product; - Execution time of about 16min/UUT; - Enclosed solution, only predefined user interaction available; - Restricted support, or at least difficult to obtain; - Further developments not possible. |  <p style="text-align: center;">Architecture of the BST station for parallel testing of 8 DUTs.</p> | <ul style="list-style-type: none"> - Similar execution time for 8 UUTs; - Improved test coverage; - Configuration options for test scenarios; - Performance analysis for session & overall execution; - Opened to further developments; - SNR validation, editable selection of test positions; - 2 similar product types analyzed in the same hardware setup. |

Why Boundary Scan (IEEE 1149.1) Testing?

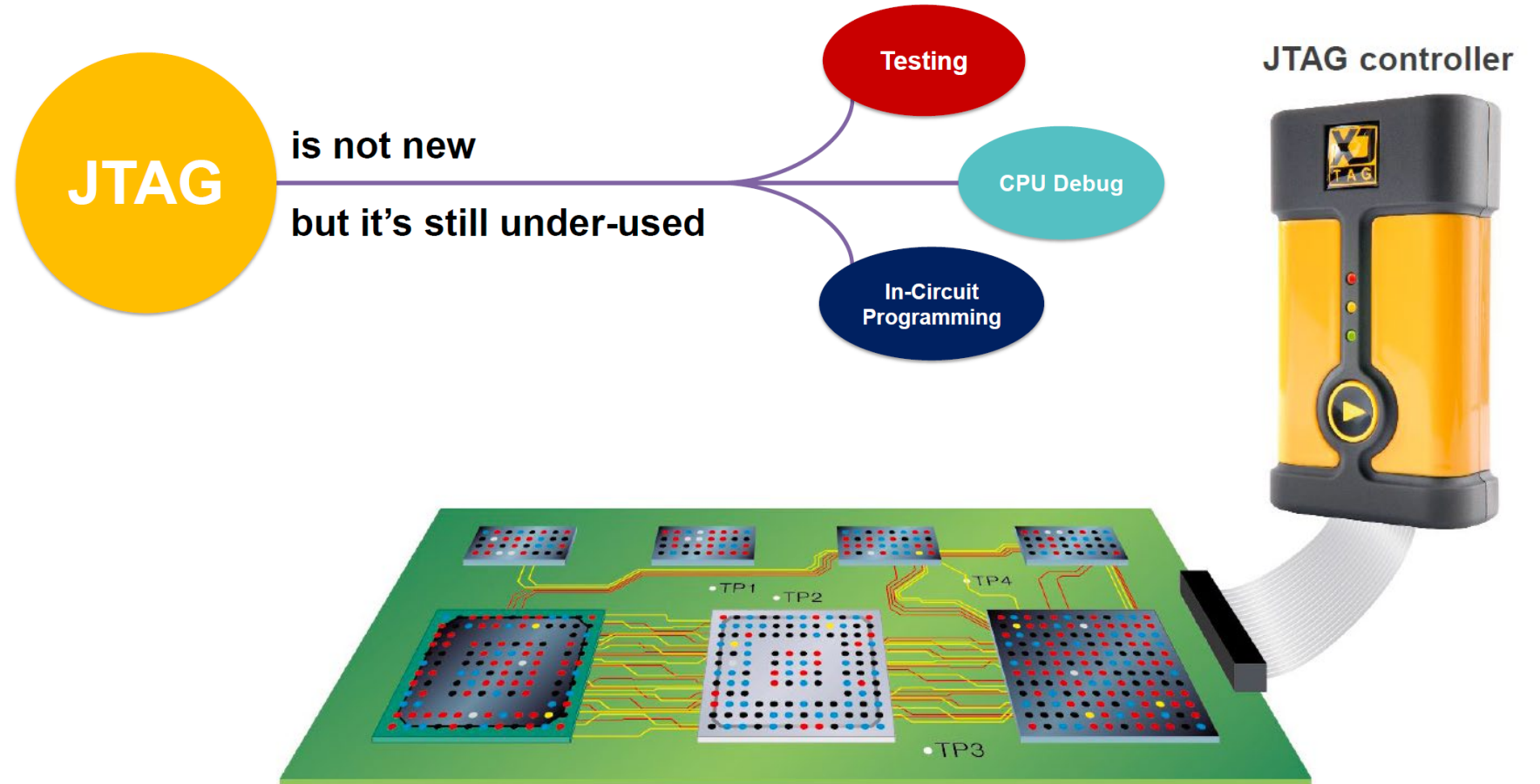
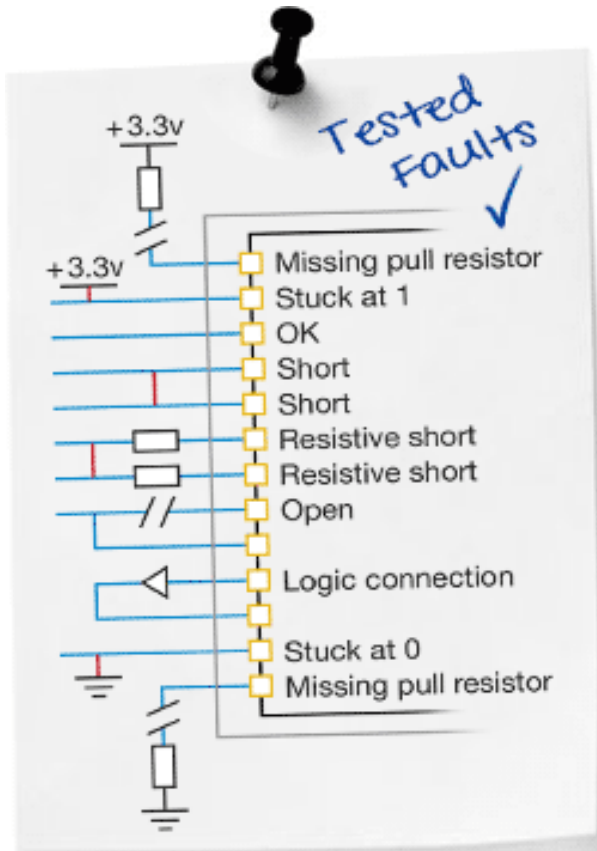
Intro concepts.

PACKAGE COMPLEXITY & TRANSISTOR
COUNT



Why Boundary Scan (IEEE 1149.1) Testing?

Intro concepts.

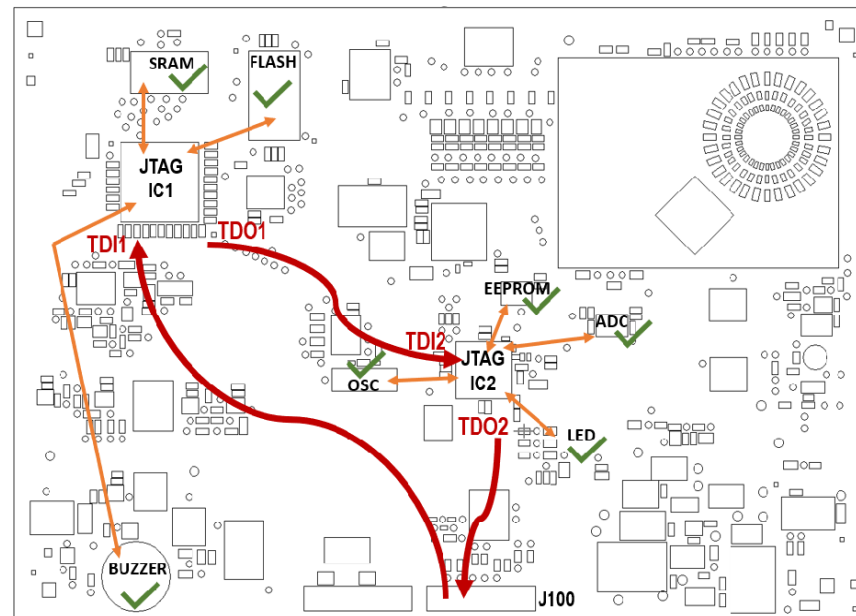
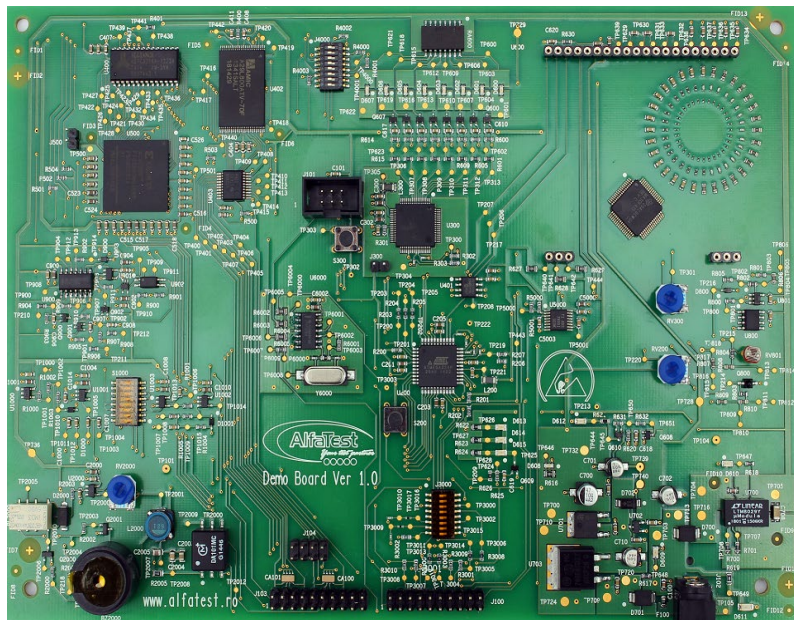


Why Boundary Scan (IEEE 1149.1) Testing?

Intro concepts.

BST minimizes access difficulties.

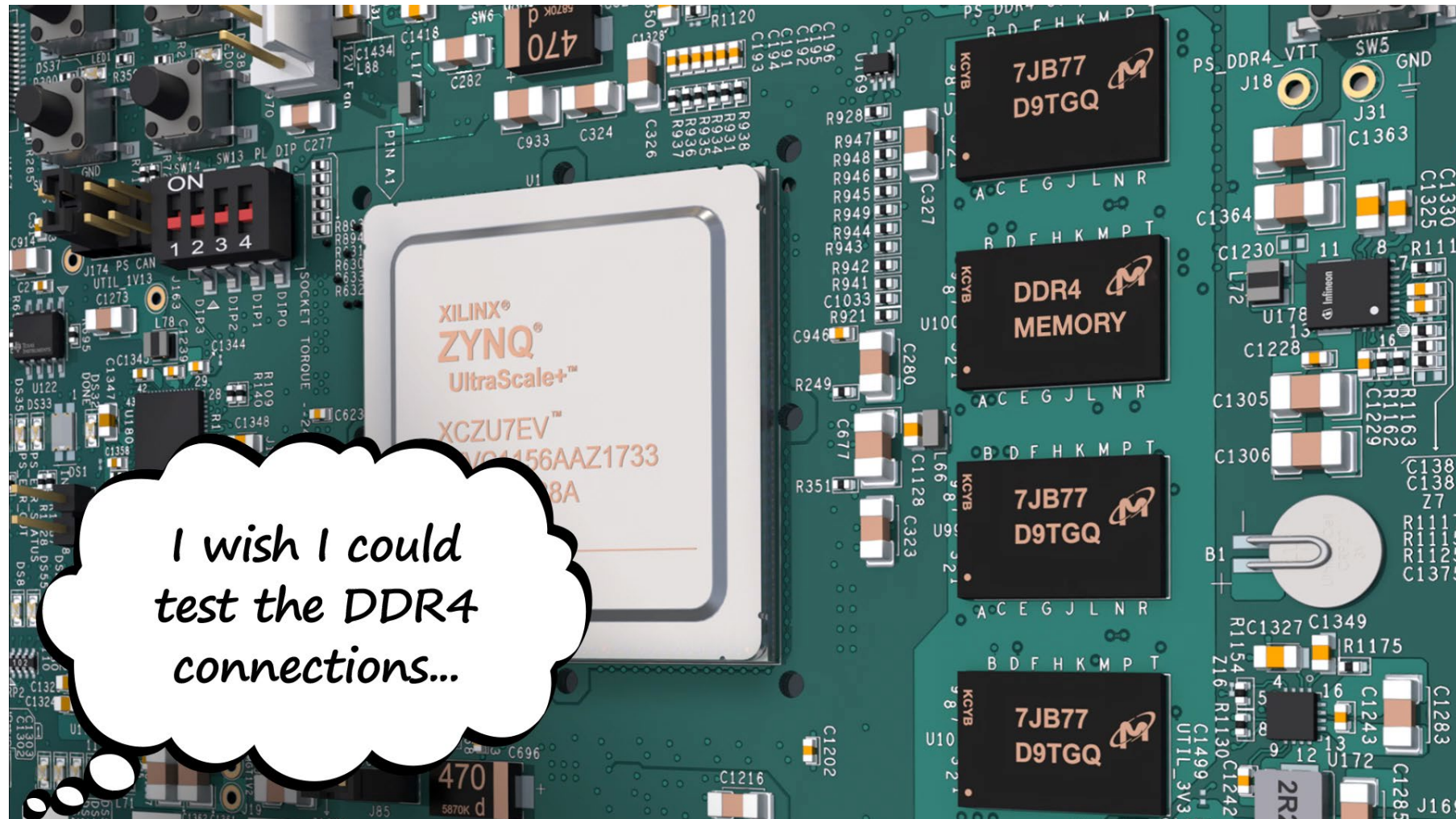
- Test Access Port interface is 4/5 signals;
- JTAG devices connect to form a chain;
- Testing of non-JTAG devices (memory chips such as DDR, SRAM, SDRAM, FLASH, EEPROM, sensors, logic circuits, switches, oscillators, LEDs etc.).



| NAME | RESULT | TIME |
|-----------------------------------|--------|---------------|
| + Check Chain Test | Passed | 0.566 |
| + Connection Test | Passed | 0.346 |
| + EEPROM Test U401 | Passed | 0.331 |
| + SRAM Test U400 | Passed | 0.072 |
| + FLASH Non Destructive Test U402 | Passed | 0.038 |
| + FLASH Test U402 | Passed | 8.486 |
| + ADC Test U5000 | Passed | 0.055 |
| + OSCILLATOR Test Y6000 | Passed | 0.165 |
| + LED Tests | Passed | 4.576 |
| + Buzzer Test | Passed | 4.581 |
| + ATMEGA Programming | Passed | 28.940 |
| TOTAL TIME | | 48.161 |

Why Boundary Scan (IEEE 1149.1) Testing?

Intro concepts.

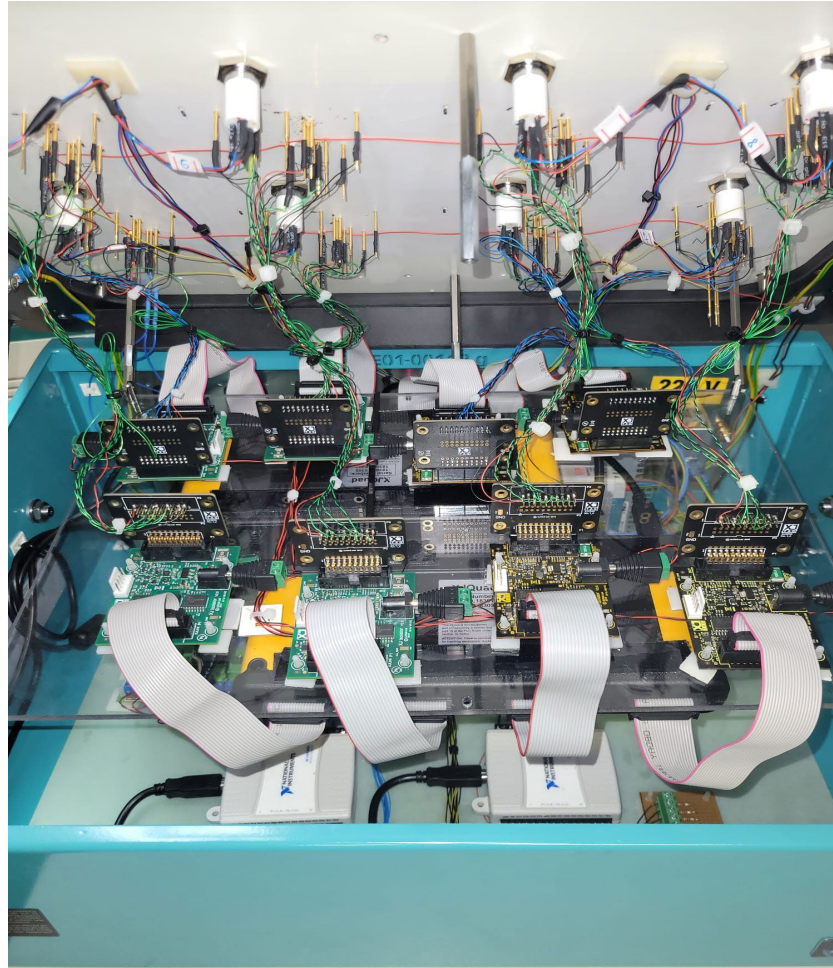


I wish I could test the DDR4 connections...

The application

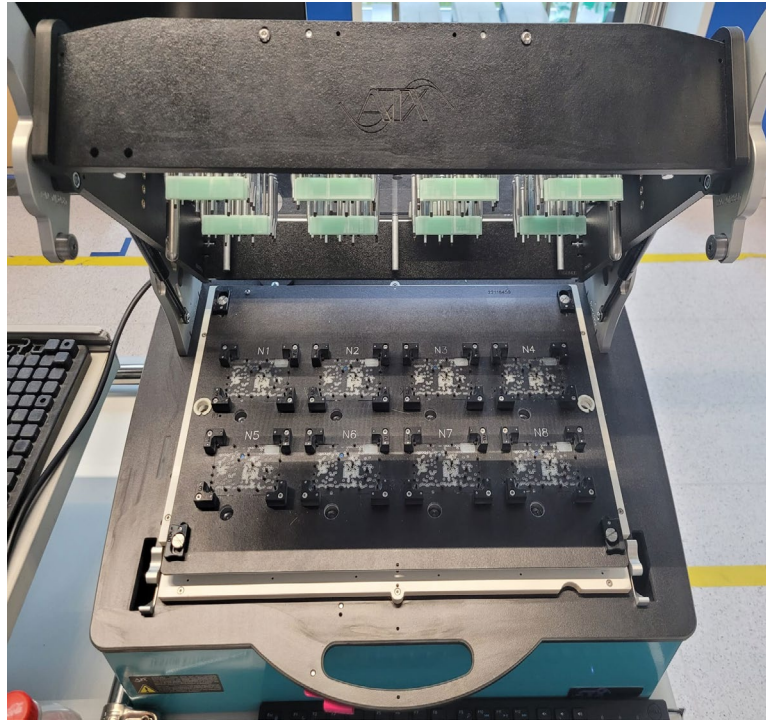
BST integration considerations.

- Parallel testing of 8 UUTs;
- 2 x XJQuad JTAG Controllers;
- 8 x XJIsolators for galvanic isolation;
- UUT power supplied by the XJQuads;
- To ensure signal integrity - cabling by twisted-pair, short wires & multiple GNDs;
- To ensure signal integrity - cabling by twisted-pair, short wires & multiple GNDs;
- Test adapter included indication of PASS/FAIL message by LEDs.



The application

BST integration considerations.



Test adapter for 8 UUTs.



A full PASS situation.



Combined PASS/FAIL situation.

The application

Deployment.

ASTEPTARE START

Project XJP: OK XJQUADS: OK

X1714500_V8_Parallel_5MHz_Extended.xjp
Project_version;CheckChain;CONNTEST;IC3.Test;
XL1.TestOscillator;XL2.TestOscillator;FlashTestNo
nDestructive;EraseAll;ProgramFlash.

Poz1-18304;Poz2-18305;Poz3-18306;Poz4-
18307;Poz5-18303;Poz6-18302;Poz7-18301;Poz8-
18300.

Sumar test

| | |
|------------------|-------|
| Total unitati: | 16 |
| Unitati PASS: | 13 |
| Unitati FAIL: | 3 |
| FPY%: | 81.25 |
| Medie/UUT (min): | 14.95 |

✔ **START TEST**

■ **INCHIDE APLICATIA**

POZITIE 1 ✔

----PASS----

```
From address 0x3ffffa to 0x3fffff  
(0x6 addresses)  
Programming complete.  
ProgramFlash passed  
>>>> TEST PASSED <<<<
```

| NAME |
|---|
| <input type="checkbox"/> Project Version |
| <input type="checkbox"/> Check Chain |
| <input type="checkbox"/> Connection Test |
| <input type="checkbox"/> SDRAM Tests |
| <input type="checkbox"/> Clock, Oscillator & Crystal Te |
| <input type="checkbox"/> Parallel NOR Flash Tests |
| <input type="checkbox"/> Flash programming |
| TOTAL TIME |

POZITIE 2 ✔

----PASS----

```
From address 0x3ffffa to 0x3fffff  
(0x6 addresses)  
Programming complete.  
ProgramFlash passed  
>>>> TEST PASSED <<<<
```

| NAME |
|---|
| <input type="checkbox"/> Project Version |
| <input type="checkbox"/> Check Chain |
| <input type="checkbox"/> Connection Test |
| <input type="checkbox"/> SDRAM Tests |
| <input type="checkbox"/> Clock, Oscillator & Crystal Te |
| <input type="checkbox"/> Parallel NOR Flash Tests |
| <input type="checkbox"/> Flash programming |
| TOTAL TIME |

POZITIE 3 ✔

----PASS----

```
From address 0x3ffffa to 0x3fffff  
(0x6 addresses)  
Programming complete.  
ProgramFlash passed  
>>>> TEST PASSED <<<<
```

| NAME |
|---|
| <input type="checkbox"/> Project Version |
| <input type="checkbox"/> Check Chain |
| <input type="checkbox"/> Connection Test |
| <input type="checkbox"/> SDRAM Tests |
| <input type="checkbox"/> Clock, Oscillator & Crystal Te |
| <input type="checkbox"/> Parallel NOR Flash Tests |
| <input type="checkbox"/> Flash programming |
| TOTAL TIME |

POZITIE 4 ✔

----PASS----

```
From address 0x3ffffa to 0x3fffff  
(0x6 addresses)  
Programming complete.  
ProgramFlash passed  
>>>> TEST PASSED <<<<
```

| NAME |
|---|
| <input type="checkbox"/> Project Version |
| <input type="checkbox"/> Check Chain |
| <input type="checkbox"/> Connection Test |
| <input type="checkbox"/> SDRAM Tests |
| <input type="checkbox"/> Clock, Oscillator & Crystal Te |
| <input type="checkbox"/> Parallel NOR Flash Tests |
| <input type="checkbox"/> Flash programming |
| TOTAL TIME |

POZITIE 5 ✔

----PASS----

```
From address 0x3ffffa to 0x3fffff  
(0x6 addresses)  
Programming complete.  
ProgramFlash passed  
>>>> TEST PASSED <<<<
```

| NAME |
|---|
| <input type="checkbox"/> Project Version |
| <input type="checkbox"/> Check Chain |
| <input type="checkbox"/> Connection Test |
| <input type="checkbox"/> SDRAM Tests |
| <input type="checkbox"/> Clock, Oscillator & Crystal Te |
| <input type="checkbox"/> Parallel NOR Flash Tests |
| <input type="checkbox"/> Flash programming |
| TOTAL TIME |

POZITIE 6 ✔

----PASS----

```
From address 0x3ffffa to 0x3fffff  
(0x6 addresses)  
Programming complete.  
ProgramFlash passed  
>>>> TEST PASSED <<<<
```

| NAME |
|---|
| <input type="checkbox"/> Project Version |
| <input type="checkbox"/> Check Chain |
| <input type="checkbox"/> Connection Test |
| <input type="checkbox"/> SDRAM Tests |
| <input type="checkbox"/> Clock, Oscillator & Crystal Te |
| <input type="checkbox"/> Parallel NOR Flash Tests |
| <input type="checkbox"/> Flash programming |
| TOTAL TIME |

POZITIE 7 ✔

----PASS----

```
From address 0x3ffffa to 0x3fffff  
(0x6 addresses)  
Programming complete.  
ProgramFlash passed  
>>>> TEST PASSED <<<<
```

| NAME |
|---|
| <input type="checkbox"/> Project Version |
| <input type="checkbox"/> Check Chain |
| <input type="checkbox"/> Connection Test |
| <input type="checkbox"/> SDRAM Tests |
| <input type="checkbox"/> Clock, Oscillator & Crystal Te |
| <input type="checkbox"/> Parallel NOR Flash Tests |
| <input type="checkbox"/> Flash programming |
| TOTAL TIME |

POZITIE 8 ✔

----PASS----

```
From address 0x3ffffa to 0x3fffff  
(0x6 addresses)  
Programming complete.  
ProgramFlash passed  
>>>> TEST PASSED <<<<
```

| NAME |
|---|
| <input type="checkbox"/> Project Version |
| <input type="checkbox"/> Check Chain |
| <input type="checkbox"/> Connection Test |
| <input type="checkbox"/> SDRAM Tests |
| <input type="checkbox"/> Clock, Oscillator & Crystal Te |
| <input type="checkbox"/> Parallel NOR Flash Tests |
| <input type="checkbox"/> Flash programming |
| TOTAL TIME |

The application

Deployment.

EXECUTIE PROIECT

Project XJP: OK XJQUADs: OK

X1714500_V8_Parallel_5MHz_Extended.xjp
Project_version;CheckChain;CONNTEST;IC3.Test;
XL1.TestOscillator;XL2.TestOscillator;Flash TestNo
nDestructive;EraseAll;ProgramFlash.

Poz1-18304;Poz2-18305;Poz3-18306;Poz4-
18307;Poz5-18303;Poz6-18302;Poz7-18301;Poz8-
18300.

Sumar test

| | |
|------------------|---|
| Total unitati: | 0 |
| Unitati PASS: | 0 |
| Unitati FAIL: | 0 |
| FPY%: | 0 |
| Medie/UUT (min): | 0 |

✔ **START TEST**

■ **INCHIDE APLICATIA**

X1714500 - Layout Viewer

File Layers View Help

Tool: Pan Selection Type: Any Find: mm Net Visibility Component Visibility

Layers

- comp_+_top
- top_paste
- top_resist
- Signal
 - top_elec
 - 0v_e_gnd
 - inner_1
 - inner_2
 - inner_3
 - inner_4
 - vdd_e_vdd
 - bottom_elec
- bottom_resist
- bottom_paste
- drill
- rout
- comp_+_bot
- Document
 - doc1
 - doc_11
 - doc_12
 - doc_13

Selectors

Nets Devices

Filter: X1714500

All Nets

X: 55.98mm Y: 2.40mm Zoom 3.4

POZITIE 4

----FAIL----

```
Analysing Logic Tests (phase 1)...  
Checking analysis: Done  
Analysing Logic Tests (phase 2)...  
  
Error on net _spi_irq5_int4_: Pull-  
up net is not pulled up properly.  
[Net Detail] [Error Detail]  
  
Error on net _spi_cs0_: Pull-down net  
is not pulled down properly.  
[Net Detail] [Error Detail]  
  
Error: Unexpected value on logic net  
_499.  
[Net Detail] [Error Detail]
```

POZITIE 8

----FAIL----

```
...Getting IC1 ID...  
Device IC1 ID :=  
0x4440301D  
...IC1 Check ID PASS...  
CheckChain passed  
  
Performing standard Connection  
Test...  
Generating Connection Test data...  
Performing Logic Tests (phase 1)...  
Performing Logic Tests (phase 2)...  
Analysing Connection Test results...  
Analysing Logic Tests (phase 1)...  
Analysing Logic Tests (phase 2)...  
  
Error on net _spi_irq5_int4_: Pull-  
up net is not pulled up properly.  
[Net Detail]
```


The application

Deployment.

ASTEPTARE START

Project XJP: OK XJQUADS: OK

X1714000_test_V2.xjp
Project_version;CheckChain;CONNTEST;IC3.Test;
XL1.TestOscillator;XL2.TestOscillator;FlashTestNo
nDestructive.

Poz1-18304;Poz2-18305;Poz3-18306;Poz4-
18307;Poz5-18303;Poz6-18302;Poz7-18301;Poz8-
18300.

Sumar test

| | |
|------------------|-------|
| Total unitati: | 188 |
| Unitati PASS: | 178 |
| Unitati FAIL: | 10 |
| FPY%: | 94.68 |
| Medie/UUT (min): | 0.02 |

START TEST

INCHIDE APLICATIA

POZITIE 1

----PASS----

```
Testing Chip Enable
Non Destructive Memory Test
PASSED...

FlashTestNonDestructive passed
>>>> TEST PASSED <<<<
```

| NAME |
|---|
| <input type="checkbox"/> Project Version |
| <input type="checkbox"/> Check Chain |
| <input type="checkbox"/> Connection Test |
| <input type="checkbox"/> SDRAM Tests |
| <input type="checkbox"/> Clock, Oscillator & Crystal Te |
| <input type="checkbox"/> Parallel NOR Flash Tests |
| TOTAL TIME |

POZITIE 2

----PASS----

```
Testing Chip Enable
Non Destructive Memory Test
PASSED...

FlashTestNonDestructive passed
>>>> TEST PASSED <<<<
```

| NAME |
|---|
| <input type="checkbox"/> Project Version |
| <input type="checkbox"/> Check Chain |
| <input type="checkbox"/> Connection Test |
| <input type="checkbox"/> SDRAM Tests |
| <input type="checkbox"/> Clock, Oscillator & Crystal Te |
| <input type="checkbox"/> Parallel NOR Flash Tests |
| TOTAL TIME |

POZITIE 3

----PASS----

```
Testing Chip Enable
Non Destructive Memory Test
PASSED...

FlashTestNonDestructive passed
>>>> TEST PASSED <<<<
```

| NAME |
|---|
| <input type="checkbox"/> Project Version |
| <input type="checkbox"/> Check Chain |
| <input type="checkbox"/> Connection Test |
| <input type="checkbox"/> SDRAM Tests |
| <input type="checkbox"/> Clock, Oscillator & Crystal Te |
| <input type="checkbox"/> Parallel NOR Flash Tests |
| TOTAL TIME |

POZITIE 4

----PASS----

```
Testing Chip Enable
Non Destructive Memory Test
PASSED...

FlashTestNonDestructive passed
>>>> TEST PASSED <<<<
```

| NAME |
|---|
| <input type="checkbox"/> Project Version |
| <input type="checkbox"/> Check Chain |
| <input type="checkbox"/> Connection Test |
| <input type="checkbox"/> SDRAM Tests |
| <input type="checkbox"/> Clock, Oscillator & Crystal Te |
| <input type="checkbox"/> Parallel NOR Flash Tests |
| TOTAL TIME |

POZITIE 5

POZITIE INACTIVA

POZITIE 6

POZITIE INACTIVA

POZITIE 7

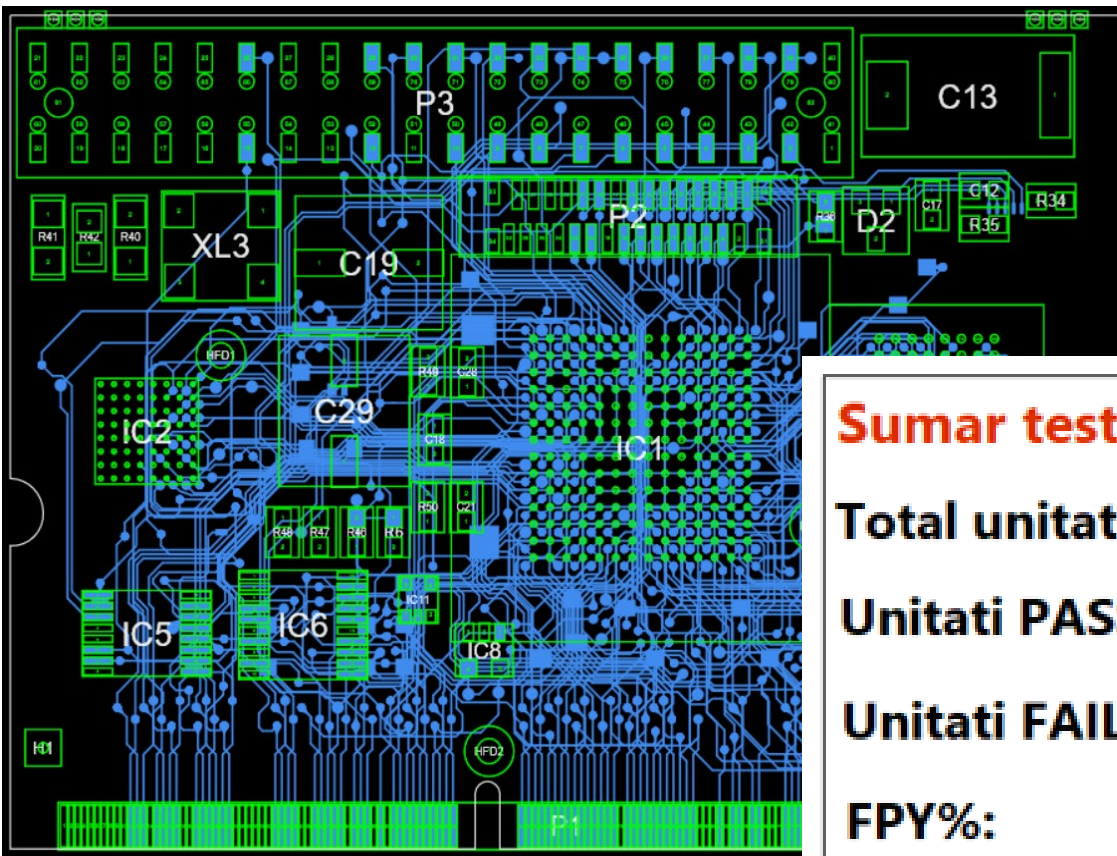
POZITIE INACTIVA

POZITIE 8

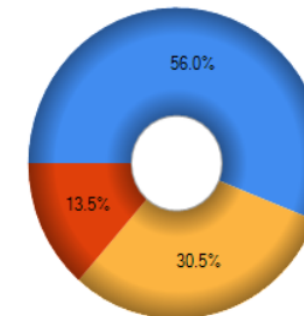
POZITIE INACTIVA

The application

Results.



| | |
|--|-----------|
| Total Number of Pins (excluding 53 unconnected pins) | 747 |
| Tested Pins | 418 56.0% |
| Power Pins | 228 30.5% |
| Untested Pins | 101 13.5% |



Sumar test

| | |
|----------------|-------|
| Total unitati: | 204 |
| Unitati PASS: | 194 |
| Unitati FAIL: | 10 |
| FPY%: | 95.10 |

■ INCHIDE APLICATIA

Sumar test

| | |
|----------------|-------|
| Total unitati: | 3286 |
| Unitati PASS: | 2595 |
| Unitati FAIL: | 691 |
| FPY%: | 78.97 |

■ INCHIDE APLICATIA

Conclusions and future work

We teach this subject at the faculty of ETcTI (4th Year, Studies in English).



Supported by:



Conclusions and future work

We teach this subject at the faculty of ETcTI (4th Year, Studies in English).

The BST project

JTAG Intro.

Look at industry study cases.

Discuss about solutions used by the local industry actors.

Design the product

We use free CAD tools (Ex. OrCAD) with a limited number of components.

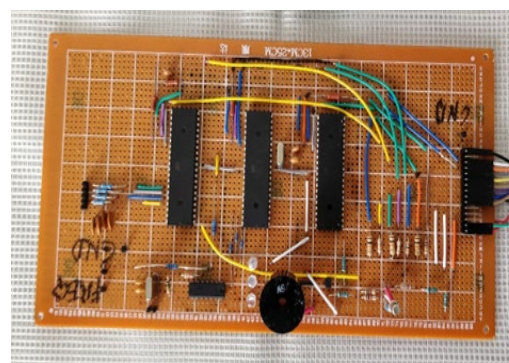
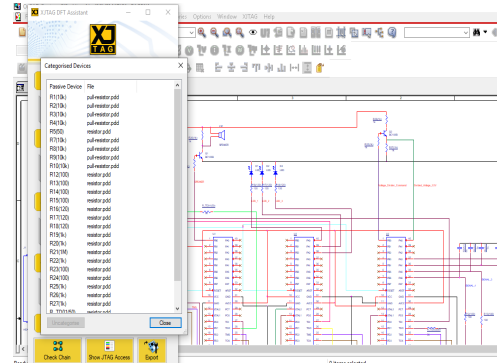
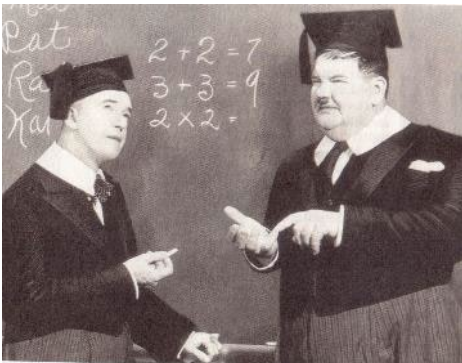
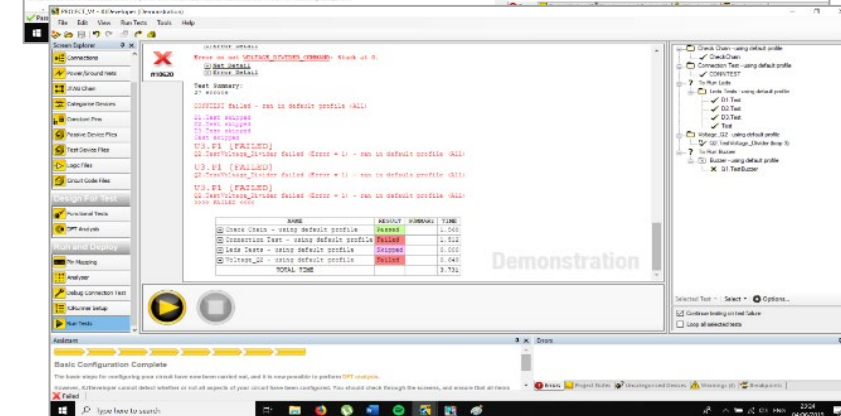
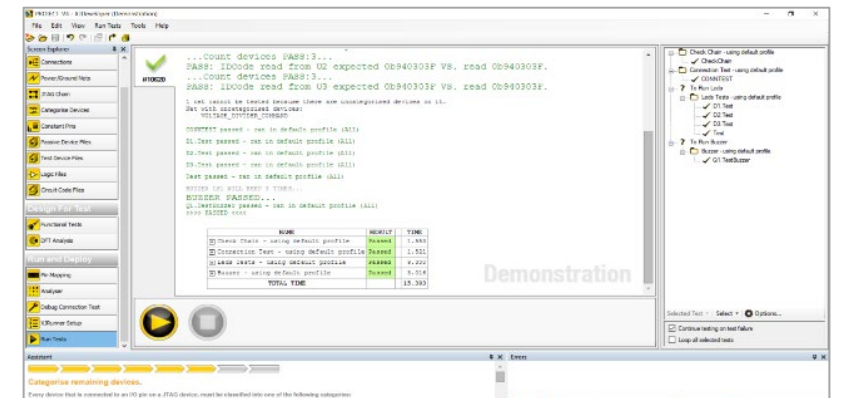
Verify product JTAG compliance by means of the XJTAG DFT Assistant free tool.

Build the product

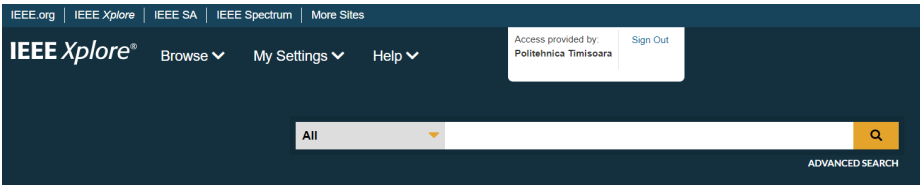
We look at the principles rather than the product complexity level.

7 Weeks/21h of study.

Testing & Validation



Conclusions and future work

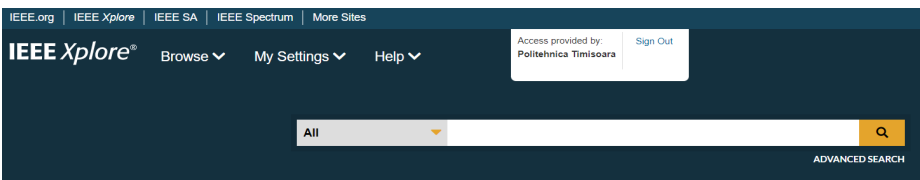


Considerations on Boundary Scan integration in industrial dedicated test stations

Publisher: IEEE Cite This PDF

Raul Ionel; Anca-Ioana Dărăbuț; Cătălin Căleanu All Authors

9 Full Text Views



Normalized Cross Correlation based Solution for Automated Optical Inspection during Boundary Scan Testing

Publisher: IEEE Cite This PDF

Raul Ionel; Anca-Ioana Dărăbuț; Cătălin Căleanu All Authors

1 Cites in Paper 31 Full Text Views

Abstract
Document Sections

Abstract:
This paper proposes a Normalized Cross Correlation (NCC) based solution for integrating automated visual inspection with Boundary Scan Test (BST, IEEE Std. 1149.1). The proposed approach can serve as a guide

IEEE Explore Papers.

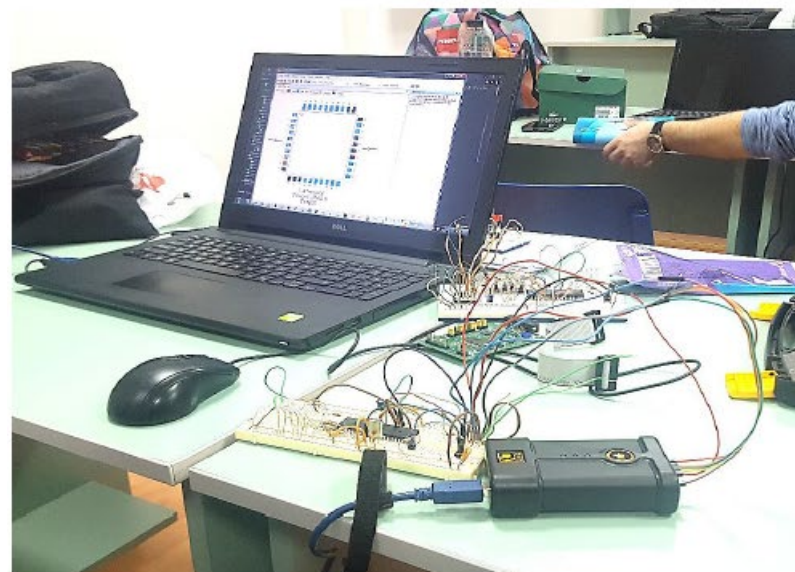


Former student Andrei Burta – presenting an industry BST solution (ISETC2022 Conference).

Conclusions and future work



Project deployment @ industry partner.



Our BST educational activity @ ETcTI.



Acknowledgement - The authors are grateful to XJTAG (xjtag.com) and Alfa Test (alfatest.ro) for the support of the Design for Boundary Scan lecture/laboratory at the Politehnica University Timișoara.



Any further questions?

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